

Switching (30V, 10A)

RES100N03

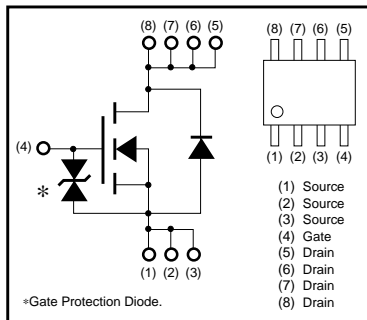
●Features

- 1) Low Qg.
- 2) Low on-resistance.
- 3) Excellent resistance to damage from static electricity.

●Structure

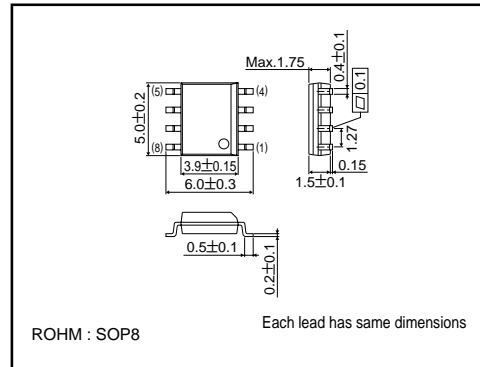
Silicon N-channel
MOS FET

●Equivalent circuit



* A protection diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use. Use a protection circuit when the fixed voltage are exceeded.

●External dimensions (Units : mm)



●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit	
Drain-Source Voltage	V _{DSS}	30	V	
Gate-Source Voltage	V _{GSS}	±20	V	
Drain Current	Continuous	I _D	10	A
	Pulsed	I _{DP} *	40	A
Reverse Drain Current	Continuous	I _{DR}	10	A
	Pulsed	I _{DRP} *	40	A
Source Current (Body Diode)	Continuous	I _S	1.3	A
	Pulsed	I _{SP} *	5.2	A
Total Power Dissipation (TC=25°C)	P _D	2	W	
Channel Temperature	T _{ch}	150	°C	
Storage Temperature	T _{stg}	-55~+150	°C	

*PW≤10μs, Duty cycle≤1%

Transistors

● Thermal resistance ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Limits	Unit
Channel to Ambient	Rth (ch-A)	62.5	$^\circ\text{C} / \text{W}$

● Electrical characteristics ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate-Source Leakage	I_{GSS}	–	–	± 10	μA	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	30	–	–	V	$I_D=1\text{mA}$, $V_{GS}=0\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	–	–	1	μA	$V_{DS}=30\text{V}$, $V_{GS}=0\text{V}$
Gate Threshold Voltage	$V_{GS(th)}$	1.0	–	2.5	V	$V_{DS}=10\text{V}$, $I_D=1\text{mA}$
Static Drain-Source On-State Resistance	$R_{DS(on)}$ *	–	10	13	m Ω	$I_D=10\text{A}$, $V_{GS}=10\text{V}$
		–	15	20		$I_D=10\text{A}$, $V_{GS}=4.5\text{V}$
		–	16	21		$I_D=10\text{A}$, $V_{GS}=4\text{V}$
Forward Transfer Admittance	$ Y_{fs} $ *	10	–	–	S	$I_D=10\text{A}$, $V_{DS}=10\text{V}$
Input Capacitance	C_{iss}	–	1600	–	pF	$V_{DS}=10\text{V}$
Output Capacitance	C_{oss}	–	900	–	pF	$V_{GS}=0\text{V}$
Reverse Transfer Capacitance	C_{rss}	–	280	–	pF	$f=1\text{MHz}$
Turn-On Delay Time	$t_{d(on)}$ *	–	17	–	ns	$I_D=5\text{A}$, $V_{DD}=5\text{V}$
Rise Time	t_r *	–	50	–	ns	$V_{GS}=10\text{V}$
Turn-Off Delay Time	$t_{d(off)}$ *	–	75	–	ns	$R_L=3\Omega$
Fall Time	t_f *	–	55	–	ns	$R_{GS}=10\Omega$
Total Gate Charge	Q_g *	–	28.5	57.0	nC	$V_{DD}=15\text{V}$
Gate-Source Charge	Q_{gs} *	–	4.9	–	nC	$V_{GS}=10\text{V}$
Gate-Drain Charge	Q_{gd} *	–	5.8	–	nC	$I_D=10\text{A}$

*Pulsed

● Body diode characteristics (Source-Drain Characteristics) ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward Voltage	V_{SD} *	–	–	1.5	V	$I_S=5.2\text{A}$, $V_{GS}=0\text{V}$
Reverse Recovery Time	t_{rr} *	–	260	–	ns	$I_{DR}=5.2\text{A}$, $V_{GS}=0\text{V}$
Reverse Recovery Charge	Q_{rr} *	–	290	–	nC	$di/dt=100\text{A}/\mu\text{s}$

*Pulsed

Transistors

●Electrical characteristic curves

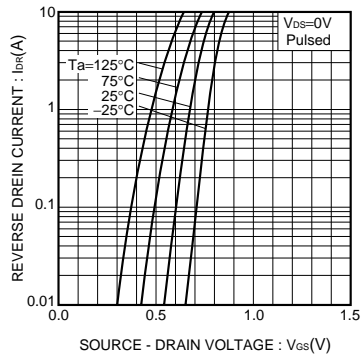


Fig.1 Reverse Drain Current vs. Source - Drain Voltage

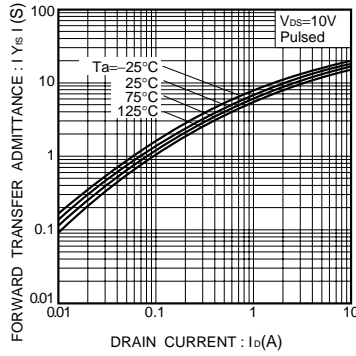


Fig.2 Forward Transfer Admittance vs. Drain Current

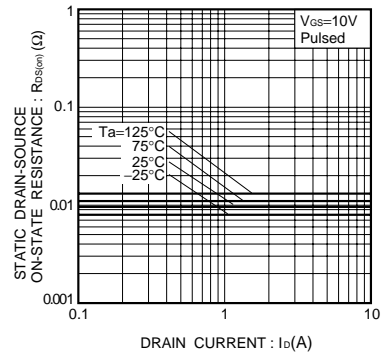


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current (I)

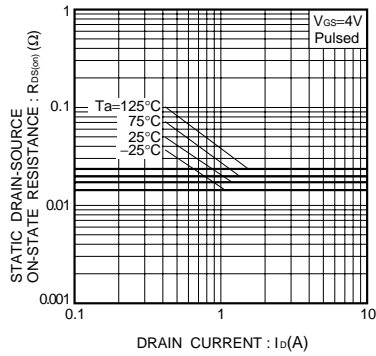


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (II)

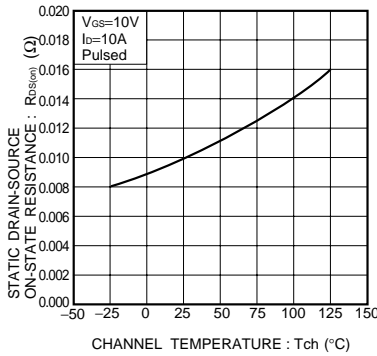


Fig.5 Static Drain-Source On-State Resistance vs. Channel Temperature

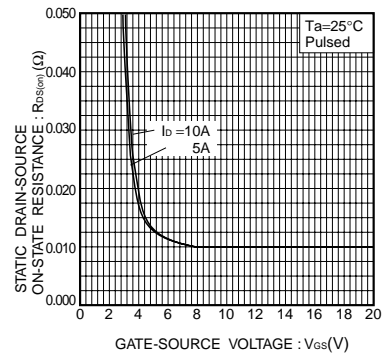


Fig.6 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

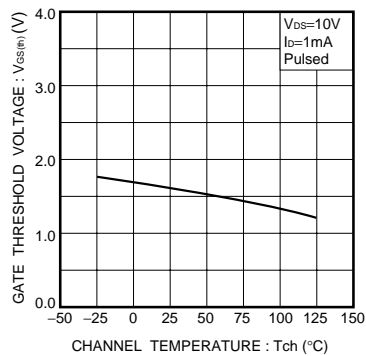


Fig.7 Gate Threshold Voltage vs. Channel Temperature

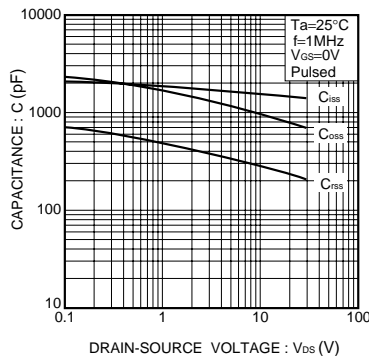


Fig.8 Typical Capacitance vs. Drain-Source Voltage

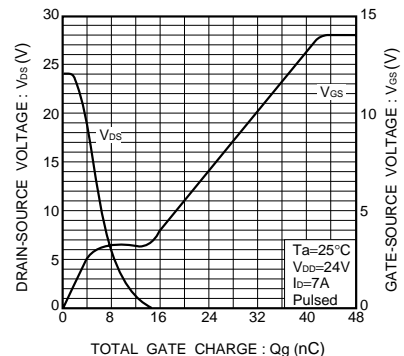


Fig.9 Dynamic Input Characteristics

Transistors

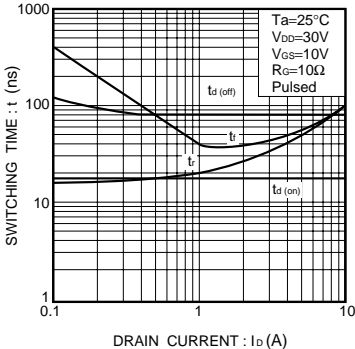


Fig.10 Switching Characteristics

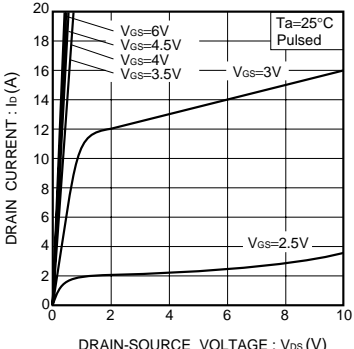


Fig.11 Typical Output Characteristics

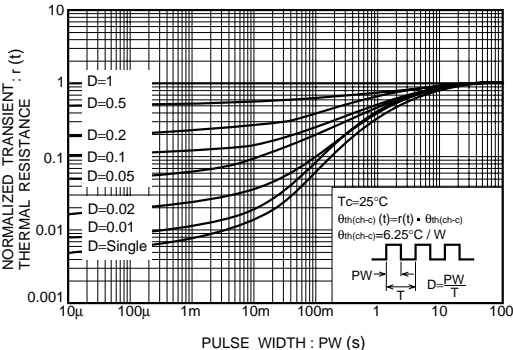


Fig.12 Normalized Transient Thermal Resistance vs. Pulse Width